3.3 V Differential Multipoint Low Voltage M-LVDS Driver Receiver

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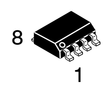
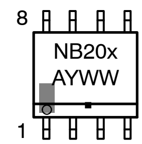


SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAM



NB20x	= Specific Device Code
x	= 0, 2, 4, 5
A	= Assembly Location
Y	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

Description

The NB3N200 is a pure 3.3 V supply differential Multipoint Low Voltage (M−LVDS) line Driver and Receiver. NB3N200S is TIA/EIA−899 compliant. NB3N200S offers the Type 1 receiver threshold at 0.0 V.

These devices has a Type−1 receiver that detect the bus state with as little as 50 mV of differential input voltage over a common−mode voltage range of −1 V to 3.4 V. The Type−1 receivers have near zero thresholds (±50 mV) and exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input.

NB3N200S supports Simplex bus configurations.

Features

- Low−Voltage Differential 30 Ω to 55 Ω Line Drivers and Receivers for Signaling Rates Up to 200 Mbps
- Type−1 Receivers Incorporate 25 mV of Hysteresis
- Meets or Exceeds the M−LVDS Standard TIA/EIA−899 for Multipoint Data Interchange
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- −1 V to 3.4 V Common−Mode Voltage Range Allows Data Transfer With up to 2 V of Ground Noise
- Bus Pins High Impedance When Disabled or $V_{CC} \leq$ 1.5 V
- M−LVDS Bus Power Up/Down Glitch Free
- Operating range: V_{CC} = 3.3 ±10% V(3.0 to 3.6 V)
- Operation from –40°C to 85°C.
- Pb−Free SOIC 8 Package
- These are Pb−Free Devices

Applications

- Low−Power High−Speed Short−Reach Alternative to TIA/EIA−485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Cellular Base Stations
- Central−Office Switches
- Network Switches and Routers

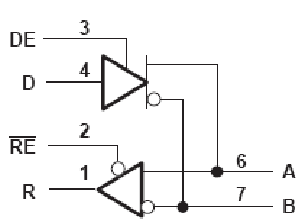


Figure 1. Logic Diagrams

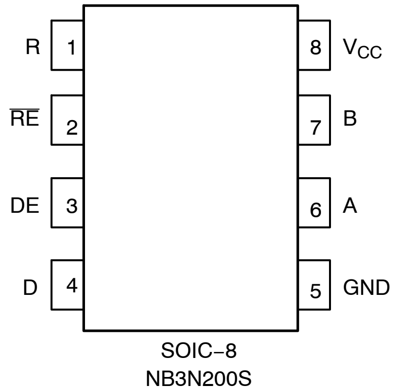


Figure 2. Pinout Diagrams (Top View)

Table 1. PIN DESCRIPTION SOIC−8

Number	Name	I/O Type	Open Default	Description
1	R	LVCMOS Output		Receiver Output Pin
2	$\overline{RE}$	LVCMOS Input	High	Receiver Enable Input Pin (LOW = Active, HIGH = High Z Output)
3	DE	LVCMOS Input	Low	Driver Enable Input Pin (LOW = High Z Output, HIGH = Active)
4	D	LVCMOS Input		Driver Output Pin
5	GND			Ground Supply pin. Pin must be externally connected to power supply to guarantee proper operation.
6	A	M−LVDS Input / Output		Transceiver Invert Input / Output Pin
7	B	M−LVDS Input / Output		Transceiver True Input / Output Pin
8	VCC			Power Supply pin. Pin must be externally connected to power supply to guarantee proper operation.

Table 2. DEVICE FUNCTION TABLE

	Inputs		Output	
	$V_{ID} = V_A - V_B$	**$\overline{RE}$**	**R**	
TYPE 1 Receiver (NB3N200)	$V_{ID} \geq 50$ mV	L	H	
	-50 mV $< V_{ID} < 50$ mV	L	?	
	$V_{ID} \leq -50$ mV	L	L	
	X	H	Z	
	X	Open	Z	
	Open	L	?	
	Input	**Enable**	**Output**	
	D	**DE**	**A / Y**	**B / Z**
DRIVER	L	H	L	H
	H	H	H	L
	Open	H	L	H
	X	Open	Z	Z
	X	L	Z	Z

H = High, L = Low, Z = High Impedance, X = Don't Care, ? = Indeterminate

Table 3. ATTRIBUTES (Note 1)

Characteristics			Value
Internal Input Pullup Resistor			50 kΩ
Internal Input Pulldown Resistor			50 kΩ
ESD Protection	Human Body Model (JEDEC Standard 22, Method A114−A)	A, B, Y, Z All Pins	±6 kV ±2 kV
	Machine Model	All Pins	±200 V
	Charged −Device Model (JEDEC Standard 22, Method C101)	All Pins	±1500 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)			Level 1
Flammability Rating Oxygen Index			UL−94 V−0 @ 0.125 in 28 to 34
Transistor Count			917 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Supply Voltage			$-0.5 \le V_{CC} \le 4.0$	V
V_{IN}	Input Voltage	D, DE, $\overline{RE}$		$-0.5 \le V_{IN} \le 4.0$	V
		A, B (200, 204)		$-1.8 \le V_{IN} \le 4.0$	
		A, B (202, 205)		$-4.0 \le V_{IN} \le 6.0$	
I_{OUT}	Output Voltage	R Y, Z, A, B		$-0.3 \le I_{OUT} \le 4.0$ $-1.8 \le I_{OUT} \le 4.0$	V
T_A	Operating Temperature Range, Industrial			−40 to ≤ +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	SOIC−8	41 to 44	°C/W
T_{sol}	Wave Solder			265	°C
P_D	Power Dissipation (Continuous)	SOIC−8	T_A = 25°C 25°C < T_A < 85°C T_A = 85°C	725 5.8 377	mW mW/°C mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS VCC = 3.3 ±10% V(3.0 to 3.6 V), GND = 0 V, T_A = −40°C to +85°C (See Notes 4, 5)

Symbol	Characteristic	Min	Typ	Max	Unit
ICC	Power Supply Current Receiver Disabled Driver Enabled $\overline{RE}$ and DE at V_{CC}, R_L = 50 Ω, All others open Driver and Receiver Disabled RE at VCC, DE at 0 V, R_L = No Load, All others open Driver and Receiver Enabled RE at 0 V, DE at V_{CC}, R_L = 50 Ω, All others open Receiver Enabled Driver Disabled RE at 0 V, DE at 0 V, R_L = 50 Ω, All others open		 13 1 16 	 22 4 24 13	mA
V_{IH}	Input HIGH Voltage	2		V_{CC}	V
V_{IL}	Input LOW Voltage	GND		0.8	V
VBUS	Voltage at any bus terminal VA, VB, VY or VZ	−1.4		3.8	V
|VID|	Magnitude of differential input voltage	0.05		V_{CC}	

DRIVER

Table 5. DC CHARACTERISTICS VCC = 3.3 ±10% V(3.0 to 3.6 V), GND = 0 V, T_A = −40°C to +85°C (See Notes 4, 5)

Symbol	Characteristic	Min	Typ	Max	Unit
DRIVER					
$\lvert V_{AB}\rvert$ / $\lvert V_{YZ}\rvert$	Differential output voltage magnitude (see Figure 4)	480		650	mV
$\Delta\lvert V_{AB}\rvert$ / $\Delta\lvert V_{YZ}\rvert$	Change in Differential output voltage magnitude between logic states (see Figure 4)	−50		50	mV
$V_{OS(SS)}$	Steady state common mode output voltage (see Figure 5)	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in Steady state common mode output voltage between logic states (see Figure 5)	−50		50	mV
$V_{OS(PP)}$	Peak−to−peak common−mode output voltage (see Figure 5)			150	mV
V_{YOC} / V_{AOC}	Maximum steady−state open−circuit output voltage (see Figure 9)	0		2.4	V
V_{ZOC} / V_{BOC}	Maximum steady−state open−circuit output voltage (see Figure 9)	0		2.4	V
$V_{P(H)}$	Voltage overshoot, low−to−high level output (see Figure 7)			1.2 V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high−to−low level output (see Figure 7)	−0.2 V_{SS}			V
I_{IH}	High−level input current (D, DE) V_{IH} = 2 V	0		10	uA
I_{IL}	Low−level input current (D, DE) V_{IL} = 0.8 V	0		10	uA
$JI_{OS}J$	Differential short−circuit output current magnitude (see Figure 6)			24	mA
I_{OZ}	High−impedance state output current (driver only) −1.4 V ≤ (VY or VZ) ≤ 3.8 V, other output at 1.2 V	−15		10	uA
$I_{O(OFF)}$	Power−off output current (0 V ≤ V_{CC} ≤ 1.5 V) −1.4 V ≤ (VY or VZ) ≤ 3.8 V, other output at 1.2 V	−10		10	uA
C_Y / C_Z	Output Capacitance VI = 0.4 sin(30E$^6\pi$t) + 0.5 V, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent)		3		pF
C_{YZ}	Differential Output Capacitance V_{AB} = 0.4 sin(30E$^6\pi$t) V, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent)			2.5	pF
$C_{Y/Z}$	Output Capacitance Balance, (C_Y/C_Z)	99		101	%
RECEIVER					
V_{IT+}	Positive−going Differential Input voltage Threshold (See Figure 11 & Tables 8 and NO TAG) Type 1 Type 2			50 150	mV
V_{IT-}	Negative−going Differential Input voltage Threshold (See Figure 11 & Tables 8 and NO TAG) Type 1 Type 2	−50 50			mV
V_{HYS}	Differential Input Voltage Hysteresis (See Figure 11 and Table 2) Type 1 Type 2		25 0		mV
VOH	High−level output voltage (IOH = −8 mA	2.4			V
VOL	Low−level output voltage (IOL = 8 mA)			0.4	V
I_{IH}	$\overline{RE}$ High-level input current (VIH = 2 V)	−10		0	μA
I_{IL}	$\overline{RE}$ Low-level input current (VIL = 0.8 V)	−10		0	μA
I_{OZ}	High−impedance state output current (VO = 0 V of 3.6 V)	−10		15	μA
C_A / C_B	Input Capacitance VI = 0.4 sin(30E$^6\pi$t) + 0.5 V, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent)		3		pF
C_{AB}	Differential Input Capacitance V_{AB} = 0.4 sin(30E$^6\pi$t) V, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent)			2.5	pF
$C_{A/B}$	Input Capacitance Balance, (C_A/C_B)	99		101	%

Table 5. DC CHARACTERISTICS VCC = 3.3 ±10% V(3.0 to 3.6 V), GND = 0 V, T_A = −40°C to +85°C (See Notes 4, 5)

Symbol	Characteristic	Min	Typ (Note 5)	Max	Unit
BUS INPUT AND OUTPUT					
I_A	Input Current Receiver or Transceiver with Driver Disabled V_A = 3.8 V, V_B = 1.2 V V_A = 0.0 V or 2.4 V, V_B = 1.2 V V_A = −1.4 V, V_B = 1.2 V	 0 −20 −32		 32 20 0	uA
I_B	Input Current Receiver or Transceiver with Driver Disabled V_B = 3.8 V, V_A = 1.2 V V_B = 0.0 V or 2.4 V, V_A = 1.2 V V_B = −1.4 V, V_A = 1.2 V	 0 −20 −32		 32 20 0	uA
I_{AB}	Differential Input Current Receiver or Transceiver with driver disabled (I_A–I_B) V_A = V_B , −1.4 ≤ V_A ≤ 3.8 V	 −4		 4	uA
$I_{A(OFF)}$	Input Current Receiver or Transceiver Power Off 0V ≤ V_{CC} ≤ 1.5 and: V_A = 3.8 V, V_B = 1.2 V V_A = 0.0 V or 2.4 V, V_B = 1.2 V V_A = −1.4 V, V_B = 1.2 V	 0 −20 −32		 32 20 0	uA
$I_{B(OFF)}$	Input Current Receiver or Transceiver Power Off 0V ≤ V_{CC} ≤ 1.5 and: V_B = 3.8 V, V_A = 1.2 V V_B = 0.0 V or 2.4 V, V_A = 1.2 V V_B = −1.4 V, V_A = 1.2 V	 0 −20 −32		 32 20 0	uA
$I_{AB(OFF)}$	Receiver Input or Transceiver Input/Output Power Off Differential Input Current; (I_A–I_B) V_A = V_B , 0 ≤ V_{CC} ≤ 1.5 V, −1.4 ≤ V_A ≤ 3.8 V	 −4		 4	uA
C_A	Transceiver Input Capacitance with Driver Disabled V_A = 0.4 sin($30E^6\pi t$) + 0.5 V using HP4194A impedance analyzer (or equivalent); V_B = 1.2 V		5		pF
C_B	Transceiver Input Capacitance with Driver Disabled V_B = 0.4 sin($30E^6\pi t$) + 0.5 V using HP4194A impedance analyzer (or equivalent); V_A = 1.2 V		5		pF
C_{AB}	Transceiver Differential Input Capacitance with Driver Disabled V_A = 0.4 sin($30E^6\pi t$) + 0.5 V using HP4194A impedance analyzer (or equivalent); V_B = 1.2 V			3.0	pF
$C_{A/B}$	Transceiver Input Capacitance Balance with Driver Disabled, (C_A/C_B)	99		101	%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. See Figure 3. DC Measurements reference.
5. Typ value at 25°C and 3.3 VCC supply voltage.

Table 6. DRIVER AC CHARACTERISTICS VCC = 3.3 ±10% V(3.0 to 3.6 V), GND = 0 V, T_A = −40°C to +85°C (Note 6)

Symbol	Characteristic	Min	Typ	Max	Unit
t_{PLH} / t_{PHL}	Propagation Delay (See Figure 7)	1.0		2.4	ns
t_{PHZ} / t_{PLZ}	Disable Time HIGH or LOW state to High Impedance (See Figure 8)			7	ns
t_{PZH} / t_{PZL}	Enable Time High Impedance to HIGH or LOW state (See Figure 8)			7	ns
$t_{SK(P)}$	Pulse Skew (|t_{PLH} − t_{PHL}|) (See Figure 7)		0	150	ps
$t_{SK(PP)}$	Device to Device Skew similar path and conditions (See Figure 7)			0.9	ns
$t_{JIT(PER)}$	Period Jitter RMS, 100 MHz (Source tr/tf 0.5 ns, 10 and 90 % points, 30k samples. Source jitter de−embedded from Output values) (See Figure 10)			3	ps
$t_{JIT(PP)}$	Peak−to−peak Jitter, 200 Mbps 2^{15}−1 PRBS (Source tr/tf 0.5 ns, 10 and 90% points, 100k samples. Source jitter de−embedded from Output values) (See Figure 10)			150	ps
tr / tf	Differential Output rise and fall times (See Figure 7)	1		1.6	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Typ value at 25°C and 3.3 V_{CC} supply voltage.

Table 7. RECEIVER AC CHARACTERISTICS VCC = 3.3 ±10% V(3.0 to 3.6 V), GND = 0 V, T_A = −40°C to +85°C (Note 7)

Symbol	Characteristic	Min	Typ	Max	Unit
t_{PLH} / t_{PHL}	Propagation Delay (See Figure 12)	2	4	6	ns
t_{PHZ} / t_{PLZ}	Disable Time HIGH or LOW state to High Impedance (See Figure 13)			10	ns
t_{PZH} / t_{PZL}	Enable Time High Impedance to HIGH or LOW state (See Figure 13)			15	ns
$t_{SK(P)}$	Pulse Skew (|t_{PLH} − t_{PHL}|) (See Figure 12) C_L = 5 pF Type 1 Type 2		 100 300	 300 500	ps
$t_{SK(PP)}$	Device to Device Skew similar path and conditions (See Figure 12) C_L = 5 pF			1	ns
$t_{JIT(PER)}$	Period Jitter RMS, 100 MHz (Source: VID = 200 mV_{pp} for 201 and 203, VID = 400 mV_{pp} for 206 and 207, V_{CM} =1 V, tr/tf 0.5 ns, 10 and 90 % points, 30k samples. Source jitter de−embedded from Output values) (See Figure 14)		4	7	ps
$t_{JIT(PP)}$	Peak−to−peak Jitter, 200 Mbps 2^{15}−1 PRBS (Source tr/tf 0.5 ns, 10% and 90% points, 100k samples. Source jitter de−embedded from Output values) (See Figure 14) Type 1 Type 2		 300 450	 700 800	ps
tr / tf	Differential Output rise and fall times (See Figure 12) C_L = 15 pF	1		2.3	ns

7. Typ value at 25°C and 3.3 VCC supply voltage. .

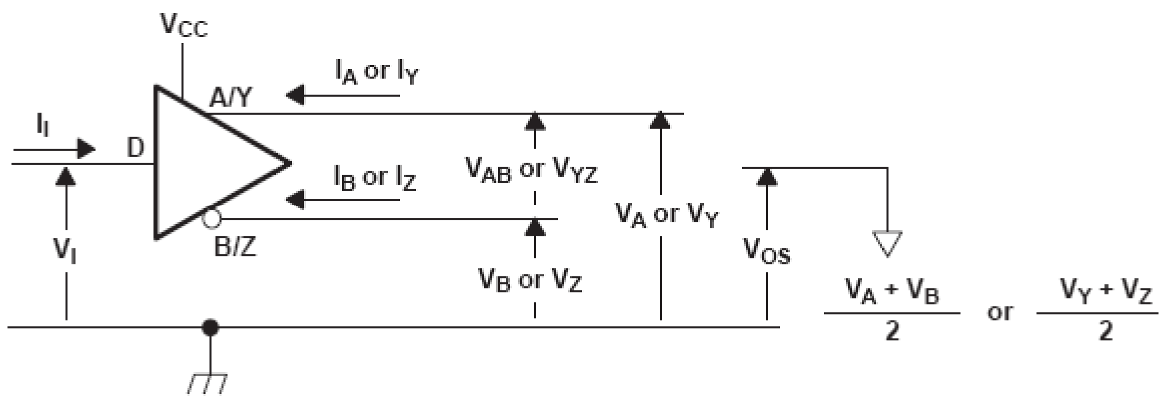
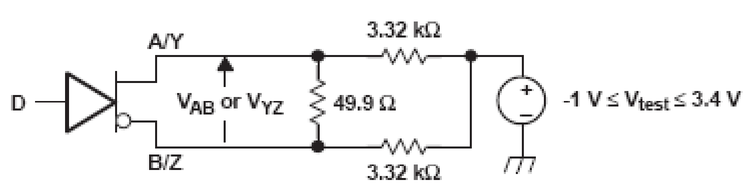
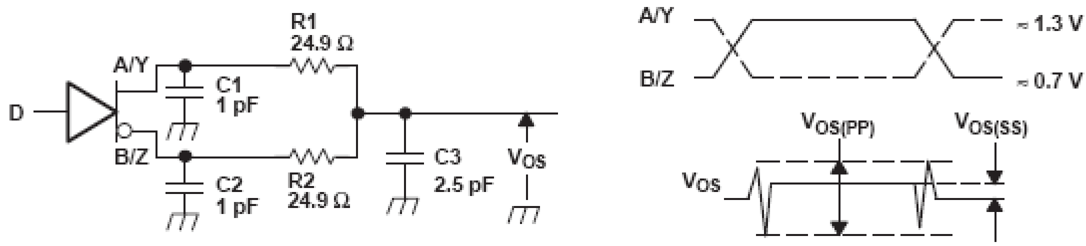


Figure 3. Driver Voltage and Current Definitions



A. All resistors are 1% tolerance.

Figure 4. Differential Output Voltage Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse frequency = 500 kHz, duty cycle = 50 ± 5%.
B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20% tolerance.
C. R1 and R2 are metal film, surface mount, 1% tolerance, and located within 2 cm of the D.U.T.
D. The measurement of $V_{OS(PP)}$ is made on test equipment with a −3 dB bandwidth of at least 1 GHz.

Figure 5. Test Circuit and Definitions for the Driver Common−Mode Output Voltage

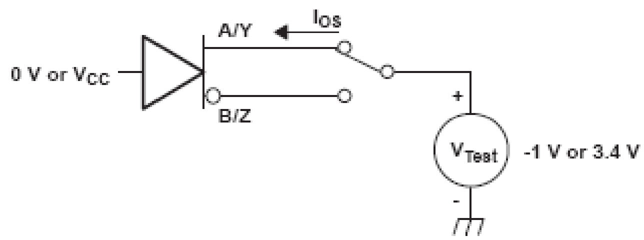
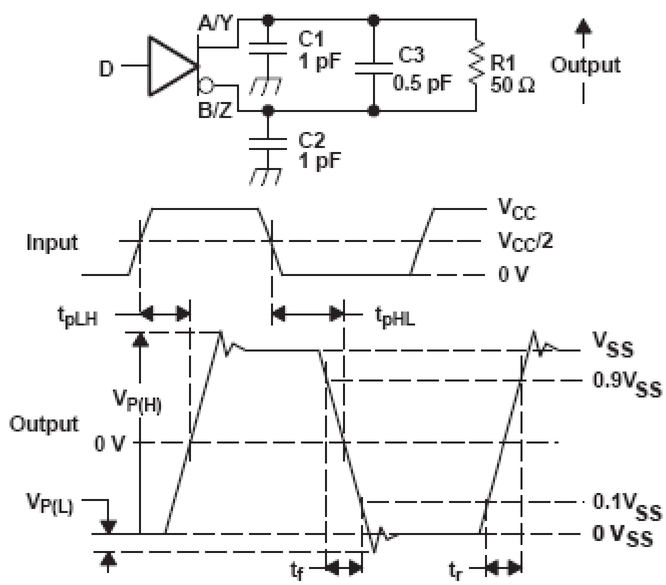
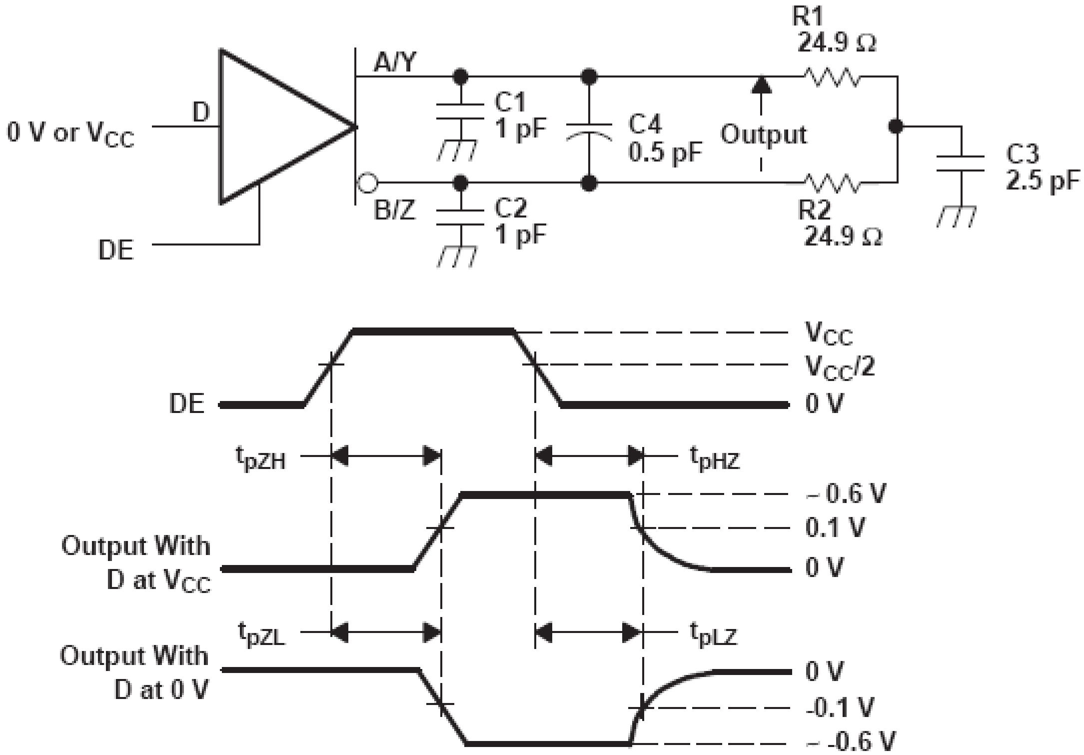


Figure 6. Driver Short−Circuit Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 500 kHz, duty cycle = 50 ±5%.
B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a −3 dB bandwidth of at least 1 GHz.

Figure 7. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, frequency = 500 kHz, duty cycle = 50 ±5%.
B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a −3 dB bandwidth of at least 1 GHz.

Figure 8. Driver Enable and Disable Time Circuit and Definitions

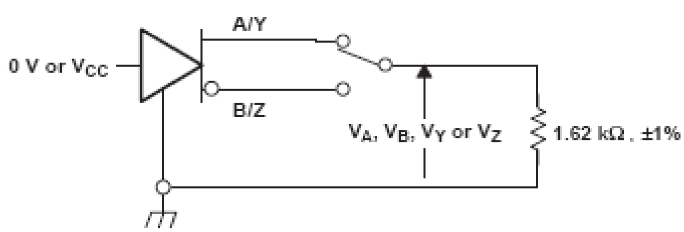
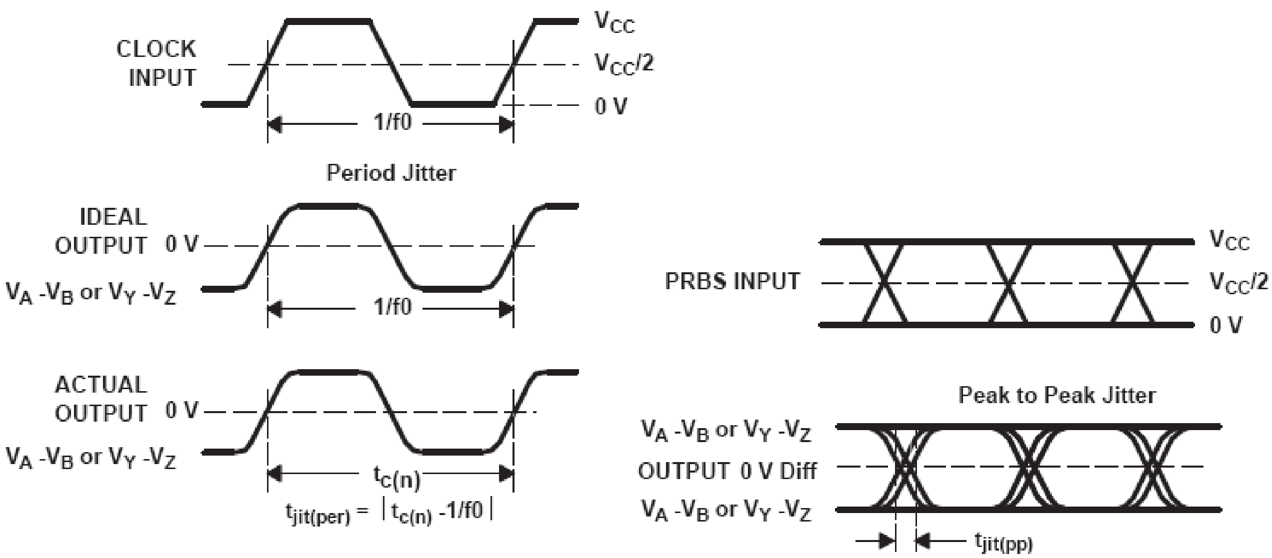


Figure 9. Maximum Steady State Output Voltage



A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
D. Peak−to−peak jitter is measured using a 200 Mbps $2^{15}-1$ PRBS input.

Figure 10. Driver Jitter Measurement Waveforms

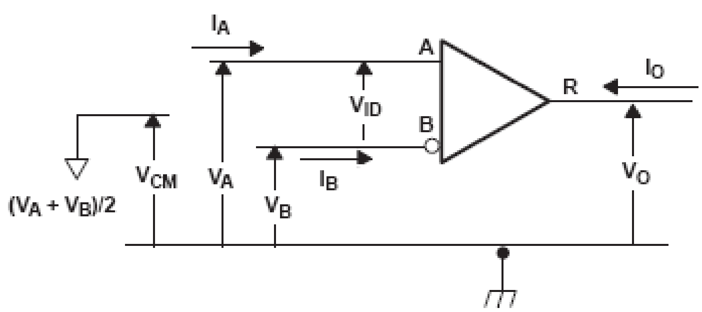
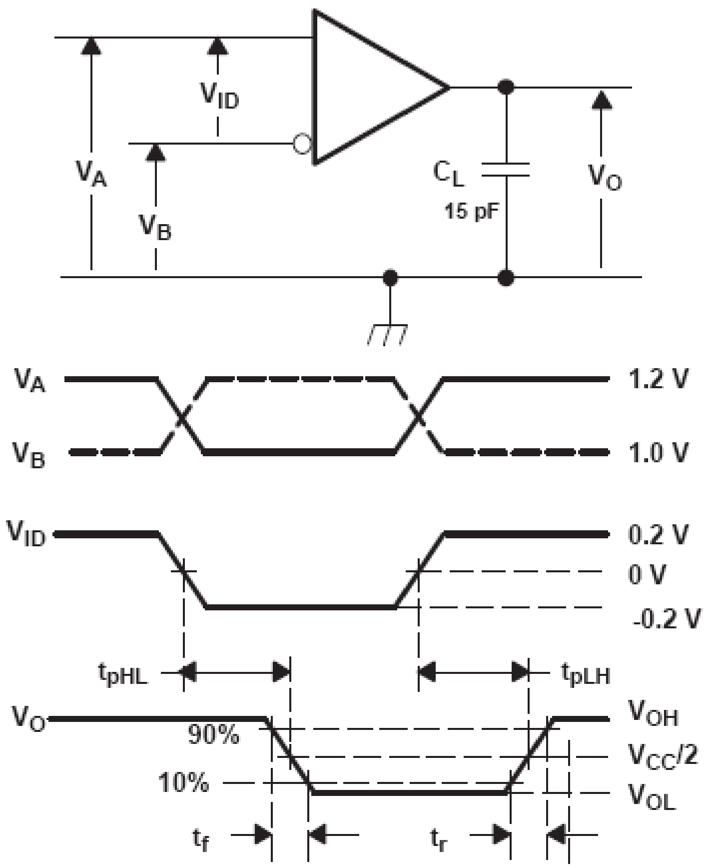


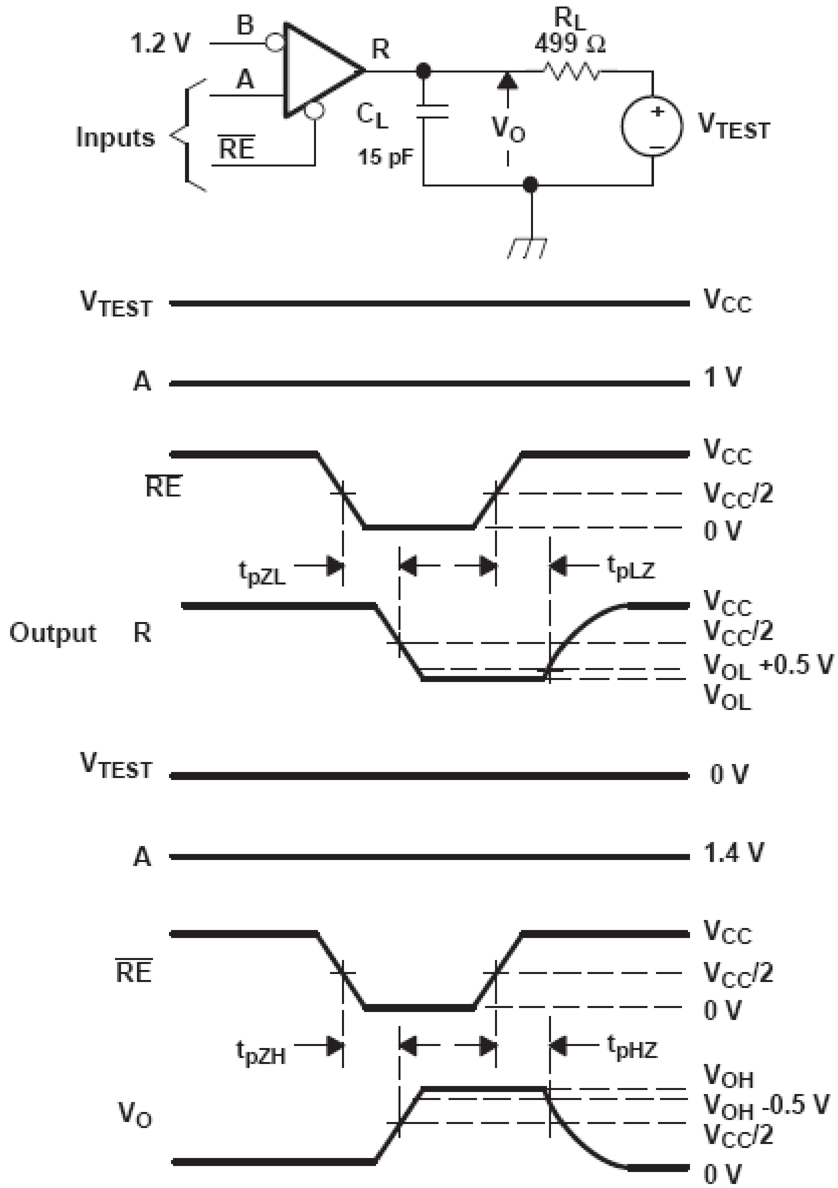
Figure 11. Receiver Voltage and Current Definitions



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 50 MHz, duty cycle = 50 ±5%. C_L is a combination of a 20%−tolerance, low−loss ceramic, surface−mount capacitor and fixture capacitance within 2 cm of the D.U.T.

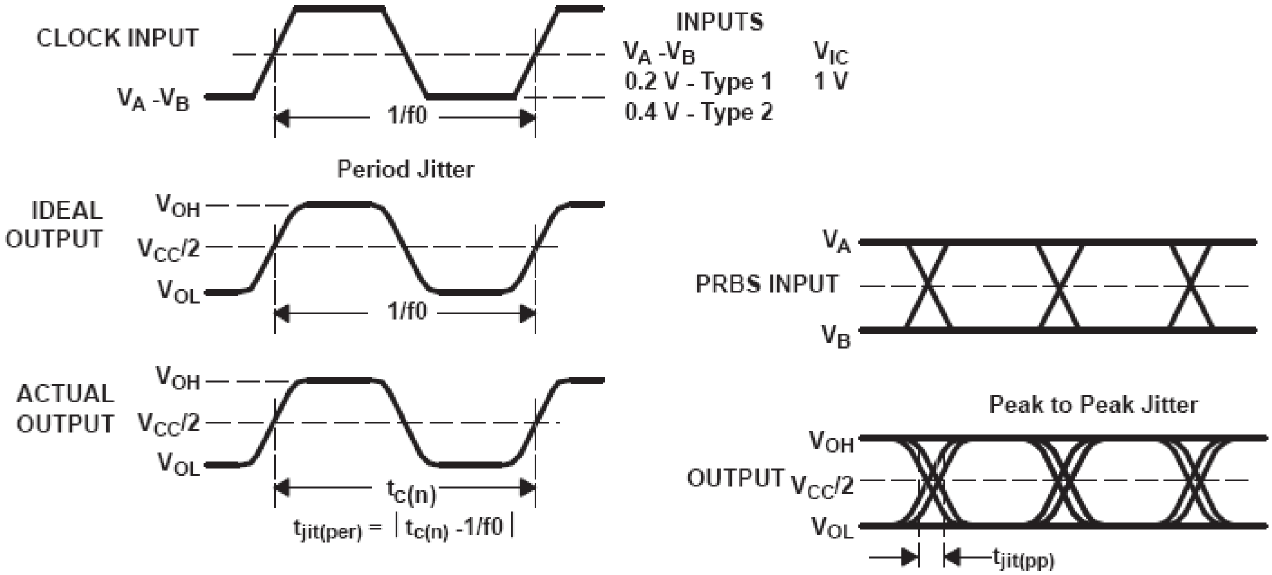
B. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 12. Receiver Timing Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, frequency = 500 kHz, duty cycle = 50 ±5%.
B. R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
C. C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and 20%.

Figure 13. Receiver Enable/Disable Time Test Circuit and Waveforms



A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
D. Peak−to−peak jitter is measured using a 200 Mbps 2^{15}−1 PRBS input.

Figure 14. Receiver Jitter Measurement Waveforms

Table 8. TYPE−1 RECEIVER INPUT THRESHOLD TEST VOLTAGES

Applied Voltages		Resulting Differential Input Voltage	Resulting Common−Mode Input Voltage	Receiver Output
VIA	VIB	VID	VIC	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.800	3.750	0.050	3.775	H
3.750	3.800	–0.050	3.775	L
–1.350	–1.400	0.050	–1.375	H
–1.400	–1.350	–0.050	–1.375	L

H = high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)

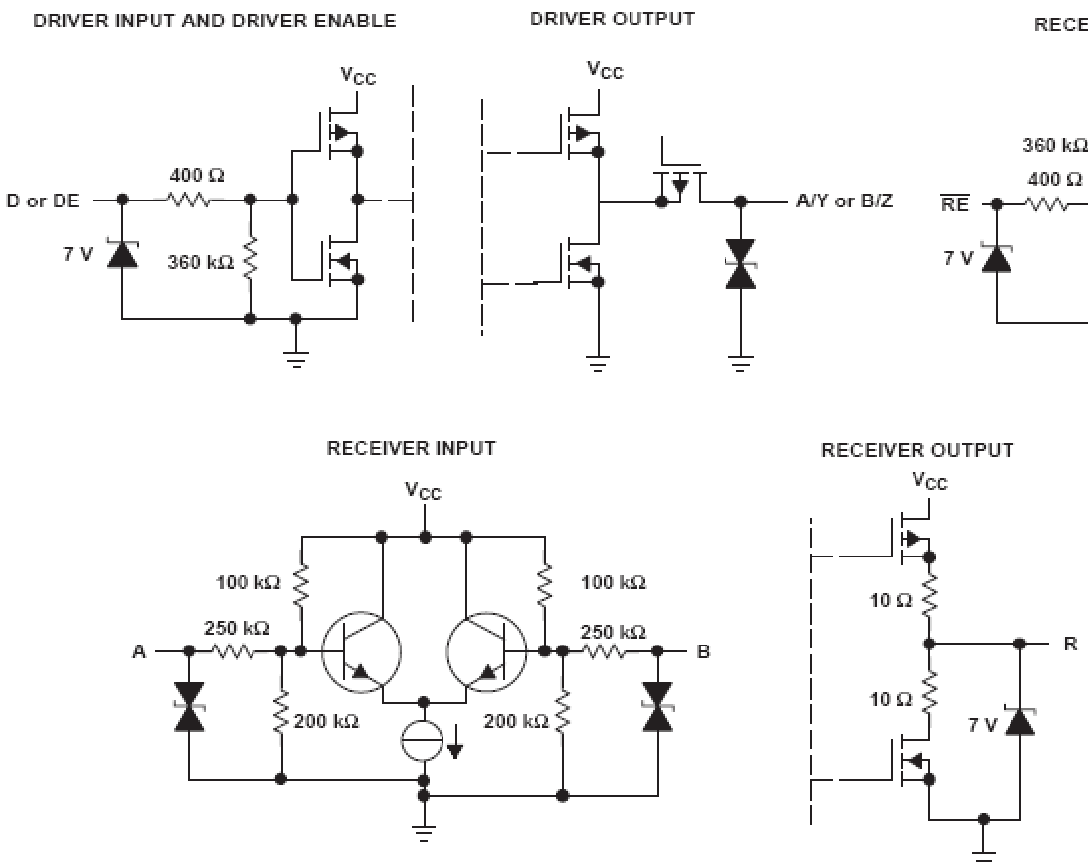


Figure 15. Equivalent Input and Output Schematic Diagrams

APPLICATION INFORMATION

Receiver Input Threshold (Failsafe)

The MLVD standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in Table 9 and Figure 16.

Table 9. RECEIVER INPUT VOLTAGE THRESHOLD REQUIREMENTS

Receiver Type	Output Low	Output High
Type 1	–2.4 V ≤ VID ≤ –0.05 V	0.05 V ≤ VID ≤ 2.4 V

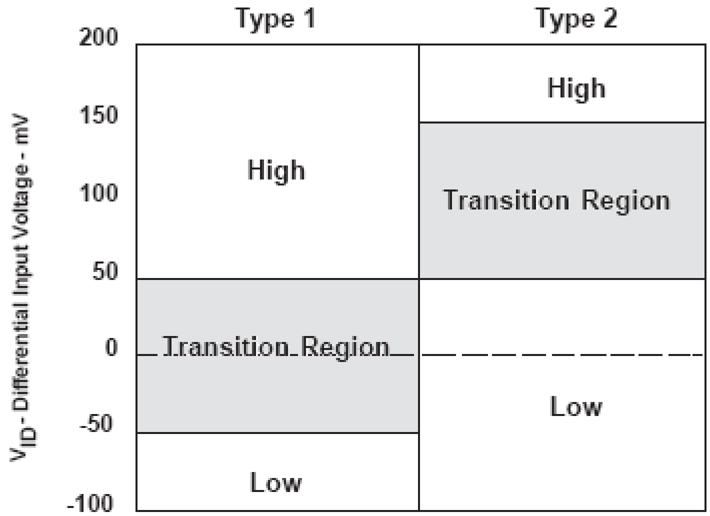


Figure 16. Receiver Differential Input Voltage Showing Transition Regions by Type

Live Insertion/Glitch−Free Power Up/Down

The NB3N200 family of products provides a glitch−free power up/down feature that prevents the M−LVDS outputs of the device from turning on during a power up or power down event. This is especially important in live insertion applications, when a device is physically connected to an M−LVDS multipoint bus and V_{CC} is ramping.

While the M−LVDS interface for these devices is glitch free on power up/down, the receiver output structure is not. Figure 17 shows the performance of the receiver output pin, R (CHANNEL 2), as V_{CC} (CHANNEL 1) is ramped. The glitch on the R pin is independent of the RE voltage. Any complications or issues from this glitch are easily resolved in power sequencing or system requirements that suspend operation until V_{CC} has reached a steady state value.

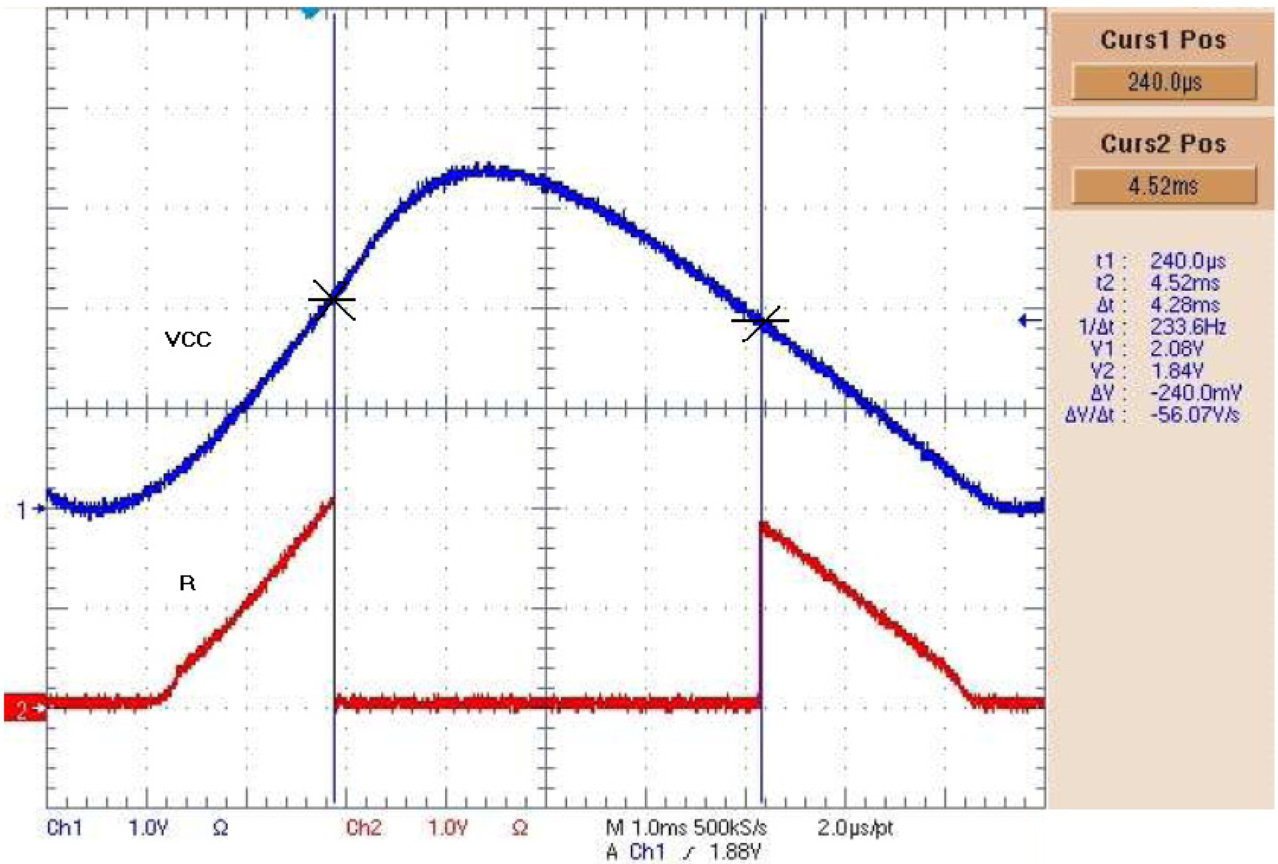


Figure 17. M−LVDS Receiver Output: VCC (CHANNEL 1), R Pin (CHANNEL 2)

Simplex Theory Configurations: Data flow is unidirectional and Point−to−Point from one Driver to one Receiver. NB3N200SDG, NB3N202SDG, NB3N204SDG, and NB3N205SDG devices provide a high signal current allowing long drive runs and high noise immunity. Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. See Figures 18 and 19. A NB3N200SDG, NB3N202SDG, NB3N204SDG, and NB3N205SDG can be used as the driver or as a receiver.

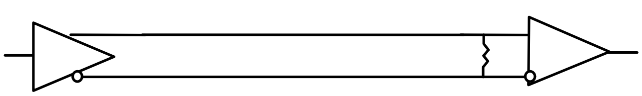


Figure 18. Point−to−Point Simplex Single Termination

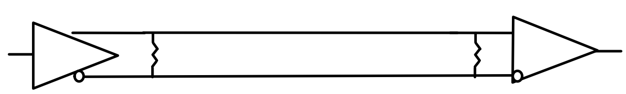


Figure 19. Parallel−Terminated Simplex

Simplex Multidrop Theory Configurations: Data flow is unidirectional from one Driver with one or more Receivers and Multiple boards are required. Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. On the Evaluation Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to a each other or a bus. See Figures 20 and 21. A NB3N200SDG, NB3N202SDG, NB3N204SDG, and NB3N205SDG can be used as the driver or as a receiver.

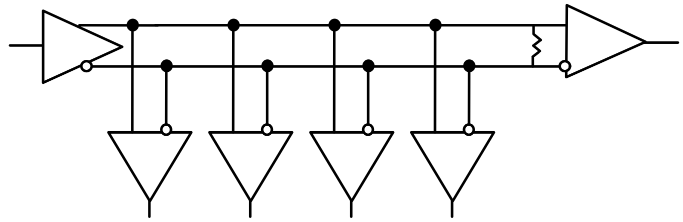


Figure 20. Multidrop or Distributed Simplex with Single Termination

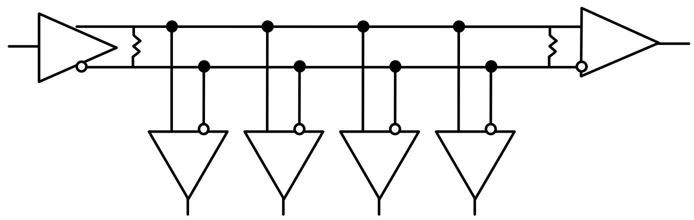


Figure 21. Multidrop or Distributed Simplex with Double Termination

Half Duplex Multinode Multipoint Theory Configurations: Data flow is unidirectional and selected from one of multiple possible Drivers to multiple Receives. One “Two Node” multipoint connection can be accomplished with a single evaluation board. More than Two Nodes requires multiple evaluation test boards. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. Parallel terminated interconnects yield typical LMVDS amplitude levels and minimizes reflections. On the Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to each other or a bus. See Figure 22. A NB3N202SDG, NB3N204SDG, and NB3N205SDG can be used as the driver or as a receiver. Full duplex bus interconnect configurations are possibe using NB3N202SDG or NB3N205SDG.

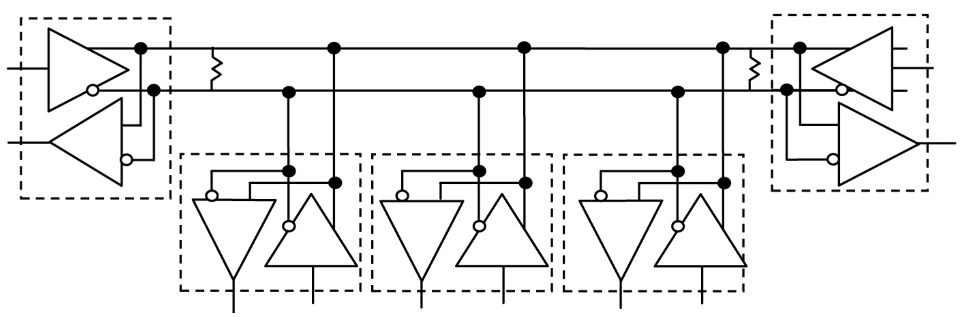


Figure 22. Multinode Multipoint Half Duplex (requires Double Termination)

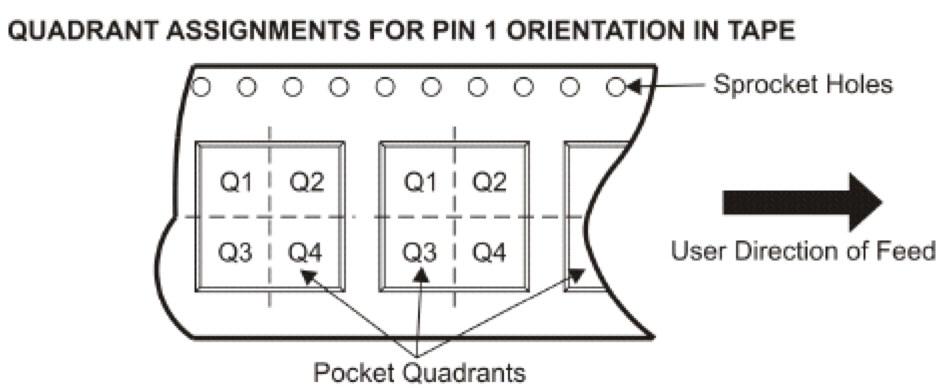


Figure 23.

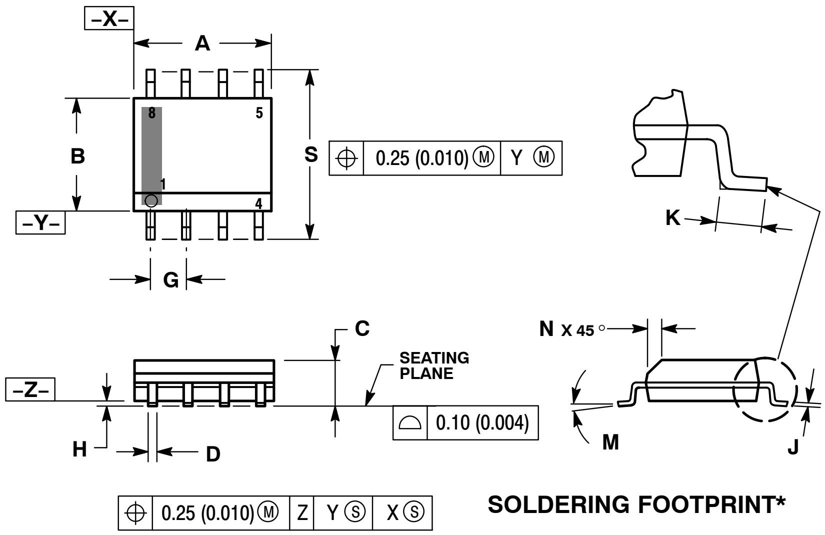
ORDERING INFORMATION

Device	Receiver	Pin 1 Quadrant	Package	Shipping†
NB3N200SDG	Type 1	Q1	SOIC−8 (Pb−Free)	98 Units / Rail
NB3N200SDR2G	Type 1	Q1	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

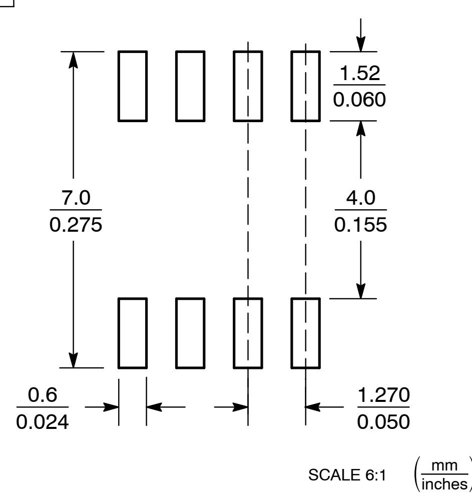
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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